COMPLETE LISTING OF CLAIMS

Claims 1-27 (canceled)

Claim 28 (previously presented): A digital to analog converter comprising:

a first current summing bus;

a second current summing bus; and

a plurality of current switches, each switch including:

a first current source for supplying a first current;

a differential pair of transistors adapted to couple said first current to either the first current summing bus or the second current summing bus in response to a pair of complementary input signals;

a pair of cascode transistors having emitters respectively coupled to the collectors of said differential pair of transistors, and collectors coupled to said first and second current summing buses, respectively; and

second and third current sources adapted to respectively supply first and second trickle currents to the emitters of said pair of cascode transistors in order to maintain said pair of cascode transistors in an 'on' state regardless of the states of said differential pair of transistors,

wherein the trickle currents are approximately 10 to 100 times smaller than said first current.

Claim 29 (previously presented): The invention of Claim 28 wherein the bases of said pair of cascode transistors are connected in common to a voltage potential.

Claims 30-32 (canceled)

Claim 33 (previously presented): The invention of Claim 28 wherein each current switch further includes a buffer transistor connected between said first current source and the common emitters of differential pair of transistors.

Claim 34 (canceled)

Claim 35 (original): The invention of Claim 28 wherein said first and second trickle currents are approximately equal.

Claim 36 (canceled)

Claim 37 (previously presented): The invention of Claim 28 wherein each current switch further includes a driver circuit for supplying said pair of complementary input signals.

Claim 38 (previously presented): The invention of Claim 37 wherein said driver circuit includes:

a fourth current source for supplying a fourth current;

a second differential pair of transistors adapted to couple said fourth current to one of the collectors of said second differential pair of transistors in response to a second pair of complementary input signals;

a second pair of cascode transistors having emitters respectively coupled to the collectors of said second differential pair of transistors;

fifth and sixth current sources adapted to respectively supply third and fourth trickle currents to the emitters of said second pair of cascode transistors in order to maintain said second pair of cascode transistors in an 'on' state regardless of the states of said second differential pair of transistors; and

two transistors having bases respectively coupled to the collectors of said second pair of cascode transistors and emitters adapted to output said pair of complementary input signals.

Claim 39 (previously presented): The invention of Claim 38 wherein said fourth current and said third and fourth trickle currents are chosen to generate a low output voltage swing at the emitters of said two transistors having bases respectively coupled to the collectors of said second pair of cascode transistors.

Claim 40 (canceled)